REMARKS

Claims 1, 2, 5, 6, 9, 10, 12, 15, 16, 19-21, 24, 25 and 28 have been amended. Claims 1-28 remain in the application.

The Examiner stated that claims 6, 12, 15, 16, 21, 24 and 25 would be allowable if amended to include limitations of base and intervening claims. Claims 6, 12, 15, 16, 21, 24 and 25 have been so amended. Claims 8 and 22 remain respectively dependent from claims 6 and 21.

Applicant has converted claims 5 and 20 to be in independent form. The Examiner rejected claims 5 and 20 under 35USC§102(b) as anticipated by Yu.

Applicant's independent claim 5 is a method claim that:
a) processes data signals through converter stages with first sets of switched capacitors,
b) interleavably generates, with a second set of switched capacitors in a selected one of the converter stages, an initial calibration signal to provide corresponding data digital codes;
c) in response to the initial calibration signal, interleavably processes downstream calibration signals with second sets of switched capacitors in downstream converter stages to provide corresponding calibration digital codes; and
d) <u>subsequently exchanges the first and second sets of switched capacitors in the selected converter stage</u>.

Applicant's independent claim 20 is an apparatus claim that recites structures. In particular, it recites a clock generator and a processor configured to command changes in clock signals of the clock generator <u>that exchange first and second sets of switched capacitors in a selected converter stage</u>.

Thus, both of claims 5 and 20 <u>exchange</u> first and second sets of switched capacitors in the selected converter stage so that the second set subsequently processes data signals and the first set is available to process calibration signals.

This important feature of Applicant's invention is supported by the filed specification. For example, page 9, lines 20-29 states,

"The second sets 60 of capacitors can now be exchanged with the first sets 50 of capacitors so that the selected converter stage and all preceding converter stages are operating in a calibrated mode.

At a subsequent time, the MDACs of the converter stages may become suspect because of various effects (e.g., temperature change or aging). The interleaved processes shown above can then be repeated to calibrate the present converter stage 44 and all preceding converter stages when they are processing calibration signals with their first sets 50 of capacitors. Once that calibration is complete, the first sets 50 are then exchanged with the second sets 60."

And page 14, lines 10-16 states,

"During the subsequent first-pair calibration period of FIG. 6, a low control signal shifts the clocks $\phi 1$ and $\phi 2$ are so that they are respectively in phase with the clocks ϕA and ϕB. This exchanges the first and second sets 50 and 60 of capacitors in the first and second operational phases of the present converter stage 44 of FIG. 3. In this arrangement, the stage can be calibrated with its first set 50 of capacitors."

Portions of the above quotations from Applicant's specification have been underlined to emphasize that the first and second sets of switched-capacitors are exchanged in the operational phases of their converter stage so that the processing of data signals is subsequently accomplished with the second set. After the first set of capacitors is calibrated, this exchange can be repeated so that processing of data signals is again accomplished with the first set.

Yu fails to teach this important feature. In contrast, Yu recites in his independent claim 6, the following processes:

a) with a first bank of capacitors, sampling a reference voltage, generating an error residual voltage, and digitizing the residual error voltage to generate a digital error value (process steps 1, 3 and 4);

b) with a second bank of capacitors, sampling an input voltage, generating, amplifying and communicating to successive converter stages a raw residual voltage, and digitizing the raw residual error voltage to generate

a <u>raw digital value</u> (process steps 2, 5 and 6); and

    c) <u>subtracting the digital error voltage from the raw digital value</u> to generate a calibrated digital output.

It must be noted that Yu names his capacitors oppositely from that of Applicant's claim 5 – that is, Yu's first and second banks of capacitors respectively correspond to the second and first sets of switched capacitors in claim 5.

In his claim 6, Yu subtracts a digital error voltage (found with his first banks) from a raw digital value (found with his second banks) to generate a digital output that corresponds to his input voltage. Yu's <u>second banks thus always process his input voltage and his first banks always process his reference voltage</u>.

Yu's teachings are also found in his summary of the invention where he states, "--- sampling a reference voltage using a first bank of capacitors --- the method then uses the stored charge from the first bank of capacitors to generate ---- an error voltage --- the error voltage can then be used to calibrate the raw value of the digitized input voltage to reduce the error gain" (column 1, line 60 to column 2, line 7). Again, Yu's first bank is only used to provide an error voltage to correct an error gain in his second bank so that Yu's <u>second banks always process his input voltage and his first banks always process his reference voltage</u>.

In contrast, Applicant's claim 5 subsequently exchanges Applicant's first and second sets of switched capacitors in Applicant's selected converter stage <u>so that Applicant's second set of switched capacitors now processes the data signals</u>.

Because Yu fails to teach the processes and structures recited respectively in Applicant's independent claims 5 and 20, he cannot anticipate these claims.

The Examiner also cited Johnson who teaches converter stages wherein, "each stage includes capacitor circuitry including first and second predetermined capacitors --- and a variable capacitance calibration capacitor" (column 2, lines 2-5). Johnson, however, <u>fails to teach</u> the use of other stage capacitors (e.g., a third and fourth capacitor) that could be exchanged with his first and second capacitors as recited in Applicant's independent claims 5 and 20. Therefore, Yu and Johnson cannot support a *prima facie* case of obviousness with respect to claims 5 and 20.

Accordingly, claims 5 and 20 patentably distinguish over the cited art. Because claims 2-4 and 7 add further limitations to claim 5 and claim 28 adds further limitations to claim 20, they also patentably distinguish over the cited art.
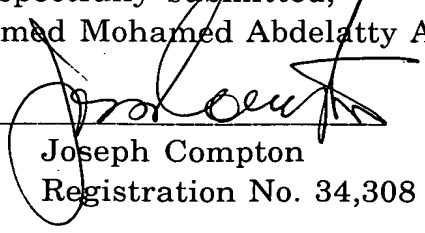
In a manner similar to that of claim 5, Applicant's independent method claims 1, 9 and 10 recite process limitations involving exchange of first and second sets of switched capacitors. Thus, they also patentably distinguish over the cited art. Because claims 13, 14, 17 and 18 add further limitations to claim 9 and claim 11 and claim 11 adds further limitations to claim 10, they also patentably distinguish over the cited art.

In a manner similar to that of claim 20, Applicant's independent claim 19 recites structure limitations involving exchange of first and second sets of switched capacitors. Thus, it also patentably distinguishes over the cited art. Because claims 23 and 26-27 add further limitations to claim 19, they also patentably distinguish over the cited art.

Because claims 5, 6, 12, 15, 16, 21, 24 and 25 have only been amended to present them in independent form and claim 20 has only been amended to present it in independent form and to clarify an antecedent reference, the reasons for their amendment are not related to patentability and therefore the amendments not alter the scope of these claims.

Applicants therefore request reconsideration and withdrawal of the rejections and an early allowance of claims 1-5, 7, 9-11, 13, 14, 17-20, 23 and 26-28 so that they join already-allowed claims 6, 8, 12, 15, 16, 21, 22, 24 and 25.

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